UNIMORE
UNIVERSITÀ DEGLI STUDI DI MODENA E REGGIO EMILIA

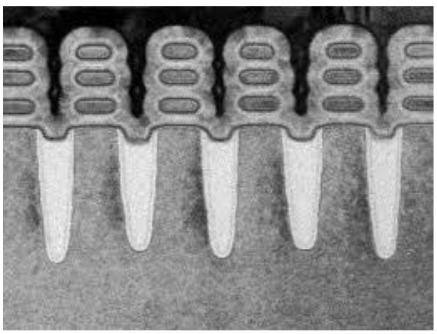
Mercoledì 22.5.2025, alle ore 14:30-16:00
Nell'edificio MO25, Aula P1.4 del DIEF
il **Prof. Souvik Mahapatra,**
Department of Electrical Engineering (**EE**),
Indian Institute of Technology di Bombay (**IITB**), Bombay, Mumbai, India
terrà un seminario dal titolo

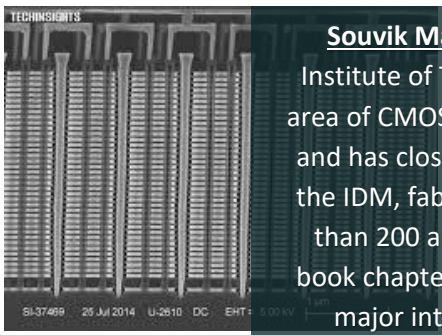
A Universal Model for CMOS Logic (BTI, SILC/TDDB, HCD) and NAND Flash Memory (P/E Cycling, DR Loss) Reliability

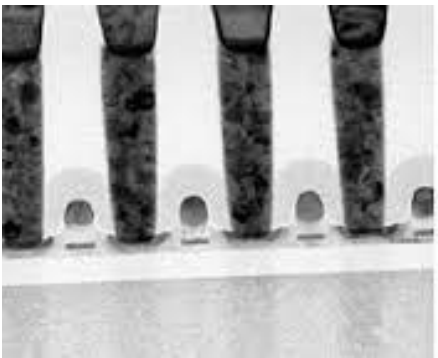
nell'ambito dei corsi di **Laurea e Laurea Magistrale in Ingegneria Elettronica / Electronic Engineering** e del **Corso di Dottorato in ICT**

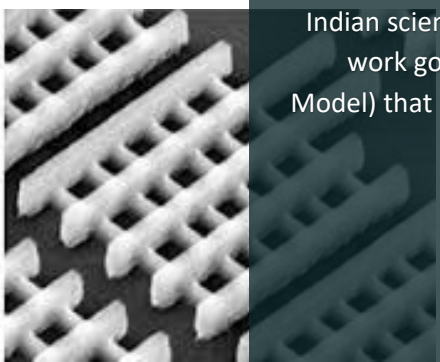
Tutti gli interessati sono invitati a partecipare

Abstract: Reliability is a key consideration for CMOS logic and NAND flash memory devices. Logic reliability can be classified as aging - where device parameters gradually shift over time or breakdown. Bias Temperature Instability (BTI), Stress Induced Leakage Current (SILC) and Hot Carrier Degradation (HCD) are manifestations of the former, while Time Dependent Dielectric Breakdown (TDDB) is the manifestation of the latter effect. NAND flash reliability primarily concerns charge loss from a programmed level (data retention (DR) loss), which gets accelerated after repeated program/erase (P/E) cycling. In this talk, we will discuss a generic framework of trap generation / passivation and trapping / detrapping, and tie up the showcased against an extensive set of measurement data.









Souvik Mahapatra is a professor of electrical engineering at Indian Institute of Technology (IIT) Bombay, Mumbai, India. He works in the area of CMOS logic device / circuit and NAND flash memory reliability, and has close collaborations with several semiconductor industries in the IDM, fab, fabless, fab-tool and EDA space. He has published more than 200 articles in peer reviewed journals and conferences, and 22 book chapters, and has delivered invited talks and tutorials at several major international conferences. He is a fellow of IEEE and several Indian science and engineering academies (INSA, INAE and IASc). His work got recognition with a named model (Mahapatra Reliability Model) that is available in Sentaurus Device simulator from Synopsys, and is being used by the semiconductor industry.